

**CLAIMS**

I claim

1. A method for determining a worst-case transition comprising:  
determining a plurality of output timing events for the plurality of input timing events based on a timing model of a gate; and  
selecting a worst-case input timing event from the plurality of input timing events based on the output timing events.
  
2. The method of claim 1, further comprising:  
determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.
  
3. The method of claim 2, wherein selecting a worst delay further comprises:  
selecting a worst delay based on the gate delays.
  
4. The method of claim 1, wherein the timing model comprises:  
$$D_g = F(S_i, C),$$
  
$$T_O = Q(T_i, D_g);$$
where  $D_g$  is a gate delay,  $T_i$  is an input slew,  $L$  is a load of the gate, and  $T_O$  is an output slew.
  
5. The method of claim 1, wherein the timing model is a timing library format (TLF) model.
  
6. An apparatus for determining a worst case transition comprising:  
means for determining a plurality of output slews for the plurality of input signals based on a timing model of a gate; and  
means for selecting a worst delay input signal from the plurality of input signals based on the output slews.

7. The apparatus of claim 6, further comprising:  
means for determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.
8. The apparatus of claim 7, wherein said means for selecting a worst delay further comprises:  
means for selecting a worst delay based on the gate delays.
9. The apparatus of claim 6, wherein the timing model comprises:  
$$D_g = F(T_i, C),$$
$$T_o = Q(T_i, D_g);$$
where  $D_g$  is a gate delay,  $T_i$  is an input slew,  $L$  is a load of the gate, and  $T_o$  is an output slew.
10. The apparatus of claim 6, wherein the timing model is a timing library format (TLF) model.
11. A computer readable medium storing a computer program comprising instructions which, when executed by a processing system, cause the system to perform a method for determining a worst case transition, the method comprising:  
determining a plurality of output slews for the plurality of input signals based on a timing model of a gate; and  
selecting a worst delay input signal from the plurality of input signals based on the output slews.
12. The medium of claim 11, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, the method further comprising:  
determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

13. The medium of claim 12, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, wherein selecting a worst delay further comprises:

selecting a worst delay based on the gate delays.

14. The medium of claim 11, wherein the timing model comprises:

$$D_g = F(T_i, C),$$

$$T_o = Q(T_i, D_g);$$

where  $D_g$  is a gate delay,  $T_i$  is an input slew,  $L$  is a load of the gate, and  $T_o$  is an output slew.

15. The medium of claim 11, wherein the timing model is a timing library format (TLF) model.